AACT: Automated Analog Coverage Tool for Mixed Signal Verification

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62 THE CHIPS TO SYSTEMS CONFERENCE

TEXAS INSTRUMENTS

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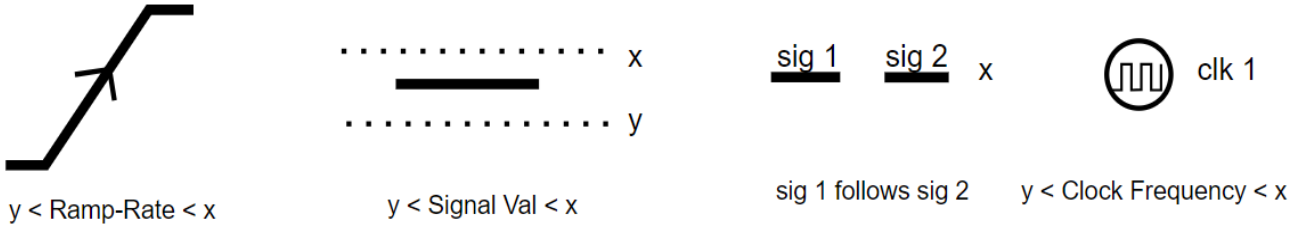
Outline:

- Motivation
- Proposed Solution
- Implementation Advantages
- Proposed Solution Details
- Results
- Conclusion

Motivation

- AMS verification methodology:
  - Involves testing and validating integrated circuits (ICs) that contain both analog and digital components.
    - Interactions among different analog IPs (SPICE models), and with different digital IPs are focus of verification
    - Guarantees adherence to functional specifications, playing a critical role in upholding the integrity and reliability of mixed-signal designs
- Limitations in existing methodology:
  - Typical low power (LP), mixed-signal (MS) SoCs Analog Mixed Signals (AMS) co-sim. cycle time accounts
    - Manual waveform reviews
    - Large Database Size
  - No existing automated framework to quantify coverage w.r.t analog properties of the design:
  - Lack of ability in System Verilog Assertions (SVA) to capture specification related to ramp, range, frequency for analog signals:

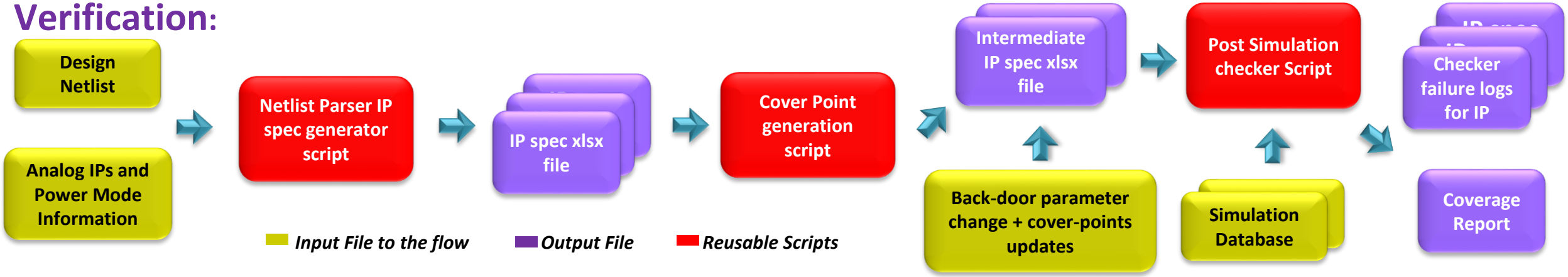


Analog Specifications

Proposed Solution

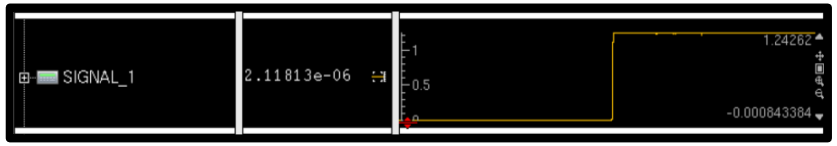
Proposed Solution

Analog-Coverage Framework for Power-Aware Verification:

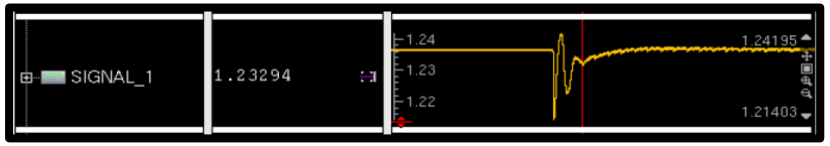


To perform a automated analysis for analog specification of signals we propose a flow to streamline and expedite verification that leverages simulation database and utilities it post runtime.

- Framework Tools: Cover point generation script, Coverage Report, Stimulus Feedback



Zoomed out



Zoomed in

- Checkers Supported:

glitch checkers, frequency glitch checkers: to flag kickback glitches and anomalous frequency variations enabled for the entire simulation time, Specifically targeted to find issues during power mode transitions.

range, frequency range, delay monitor, comparator, ramp checkers : to monitor deviation from the general behavior

Implementation Advantages

- Complete Coverage Across Power Modes: Ensures all possible analog signal scenarios are captured during different power states and in between transitions.
- SoC Power Mode Management: Based on type of ports and specifications we generate different kinds of checks for each power mode and considers the scenario covered if the checkers are enabled and passed.
- Regression Level Analysis: This helps determine if key analog behaviour are exercised in the simulations and aids us in identifying missing scenarios, allowing targeted stimulus generation for improved coverage for a holistic verification
- No Impact on Simulation Runtime: The checks are introduced in a post processing stage, ensuring they do not interfere with the core simulation execution.
- Highly Scalable: The proposed flow at different stages of integration like IP, Sub-System, SoC level.
- Independent of Modeling Approach: The proposed flow works seamlessly regardless of whether the IP is kept as a SPICE or a Analog Behavioural Model (ABMOD).

Proposed Solution Details

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AACT Spec file

Automated addition of checkers based on type of port:

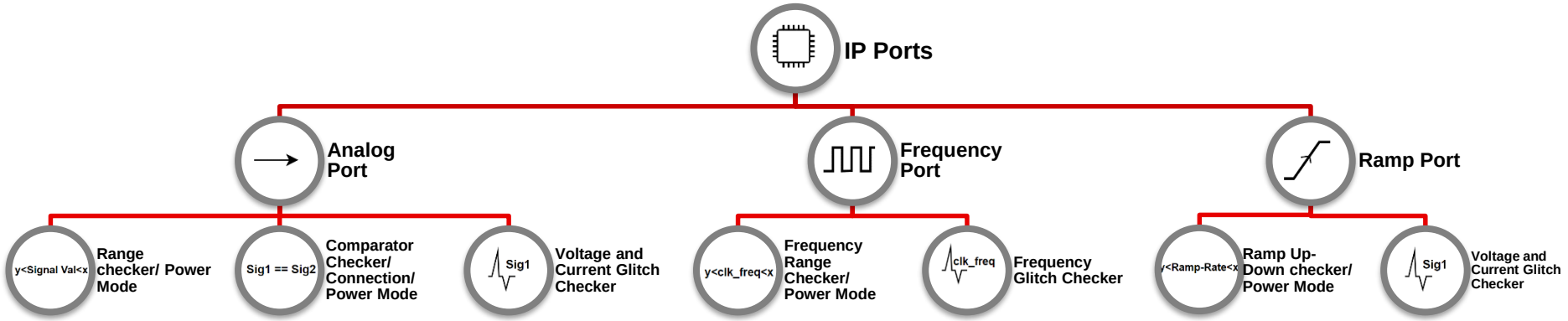
- The framework extracts port information and expected behaviour across power modes by parsing the netlist, leveraging: naming convention, performance requirement documents.
- Using the input information preliminary nominal values, frequency and ramp rates are assigned to ports for different power modes.
- Spec File Utilization: Generated spec file is fed to the cover-point generator, which automatically creates cover bins based on port type. Nominal value serve as input parameters for coverage analysis.
- User Interaction & Customizations: The generated intermediate IP spec file allows user to tweak parameters or add more cover bins, providing a flexible interface

Hierarchical path:	***Path from IP instance in testbench***						
Default Mode Enable Condition:	***Default Power Mode 1 Enable Sequence***	***Default Power Mode 2 Enable Sequence***	***Default Power Mode 3 Enable Sequence***	***Acceptable Percentage Variation for Glitches:***	***2***	***Default Delay for Checker Enable:***	***10***
Port Name	***Power Mode 1 (Active)***	***Power Mode 2 (Standby)***	***Power Mode 3 (Shutdown)***	***Port Type (Analog/Frequence/Ramp)***	***Signal to compare***	***Acceptable Voltage Deviation***	***0.001***
Port 1	***1.58 (V/I)***	***1.58***	***0***	***Analog***	***Signal Paths for comparator check extracted from netlist***	***Acceptable Current Deviation***	***1.00E-07***

Flow Generated IP level Spec File

Cover Point Addition Scheme

- Analog Ports:
  - We verify the signal generated or consumed by the IP is within expected range for different power modes using the range checker bins.
  - To ensure connectivity with the rest of the design comparator checker bins are added check if there is no anomalous drops in signal level due to issues in connection
  - We add glitch checker bins that monitor for unexpected spec violating spikes in voltage or current through out the simulation time and during power mode transitions.
- Frequency Ports:
  - To check the functionality of clock generators we add frequency range checkers to monitor clock at different power modes and trim values.
  - To check the fidelity of the generated clock we add frequency glitch checker to find an issue during power mode transitions.
- Ramp Ports:
  - To check if certain signals meet the performance requirements and have acceptable Ramp-Rate we add Ramp checkers
  - To monitor for spikes during ramping we add glitch checker bins on these ports



Results

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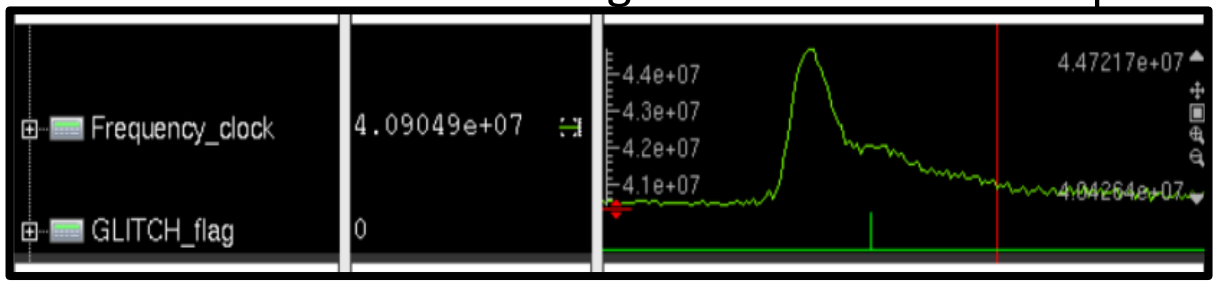
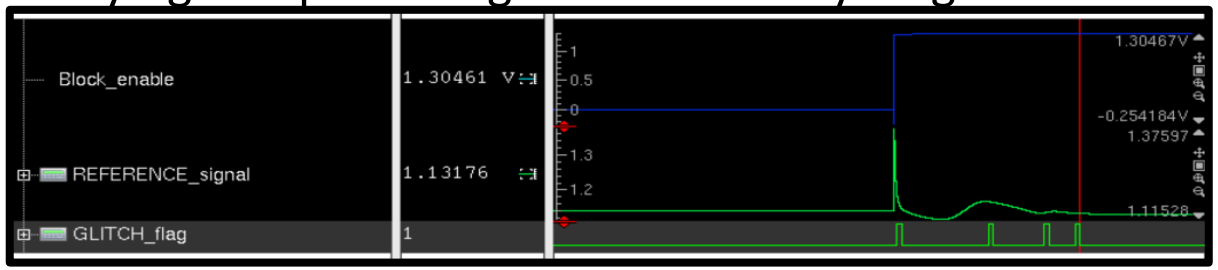
Evidence

- The developed automated analog coverage tool is proven effective and could be utilized in mixed signal SoC for expedited potential issue screening.
- For core analog IPs such as oscillator and reference generators having **8** and **6** ports for which, AACT added **26** and **16** checker points to validate the functionality and quality of stimulus.
- The failures from the tool generated checker helps in identifying complex design issues in early stages.



Issue 1: Frequency overshoot

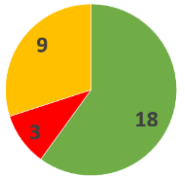
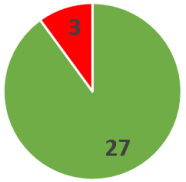
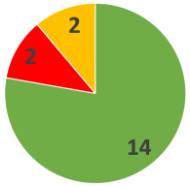
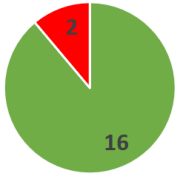
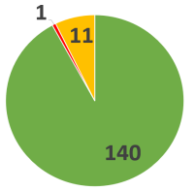


Issue 2: Reference Kickback

- The tool successfully pinpointed deficiencies in the current test suite, delivering actionable insights that informed targeted enhancements to stimulus generation, ultimately strengthening overall test effectiveness.

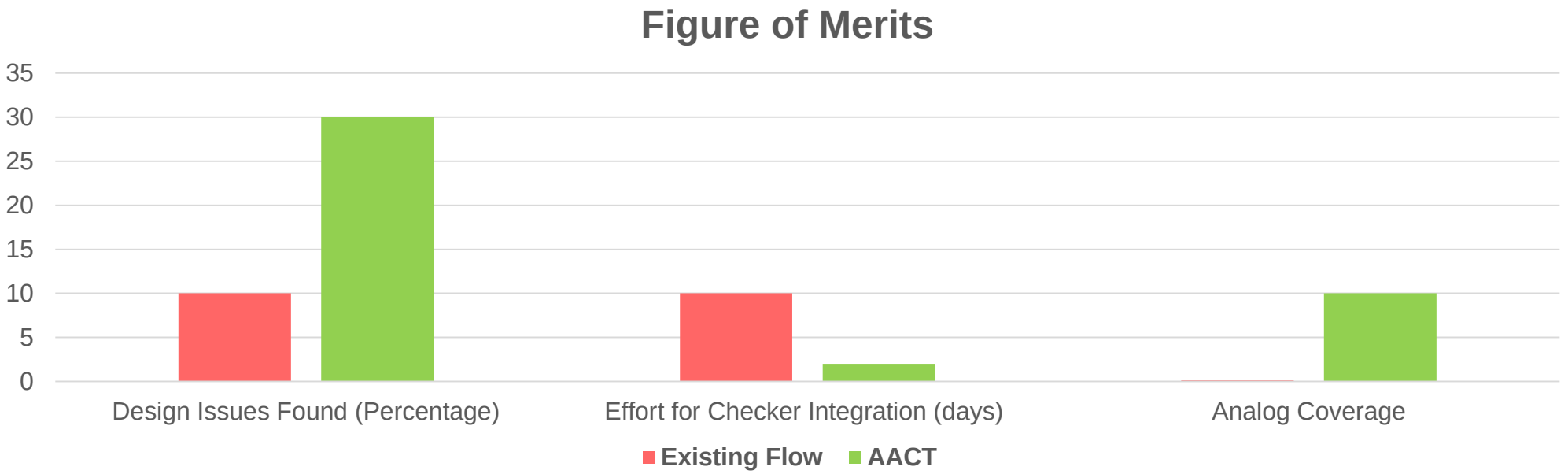
AACT interception Summary

Passed Failed Inactive

Regression	DUV	Regression Metrics				Failure Analysis	Issues in Design
		Total Checkers		Coverage			
		Auto Added	Manually Added	Original Stimulus	Updated stimulus		
IP AMS	***Oscillator***	26	4			Variation in the oscillator frequency observed during switching the reference supply	Timing violation
	Analog IP	16	2			IP causing a kickback on the current references when enabled, impacting memory references	Memory access corruption
SoC AMS	***Mixed Signal SoC***	134	18			Coupling issues in oscillators sharing the same reference buffer leading to a noisy frequency	Variation causing incorrect real-time clock output

Conclusion

- Automated Analog Coverage Tool: We introduce a scalable and efficient framework for enhancing the verification and tracking of analog IPs focusing on comprehensive coverage across power modes.
- Analog Functional Coverage: We present a first of its kind, automated analog property centric verification quantification flow in a highly digital dominated framework.
- Robust Framework: Mapping based on type of port ensures a systematic creation of range, frequency, ramp, glitch checks tailored to their unique characteristics.
- Stimulus Evaluation: Auto addition of basic checkers, helps identify gaps in stimulus, ensuring that all critical scenarios are exercised
- Flexibility: The flow is flexible, allowing user customization for fine tuning verification parameters.



Questions

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